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10/695,606	10/28/2003	Lee Doyle Whetsel JR.	TI-14996D.4	6309

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EXAMINER	
BAKER, STEPHEN M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,606	WHETSEL ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-36 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-36 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

S.O.O.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because "without having to repetitively cycle through multiple shift operations" apparently should be "without having to repetitively cycle through multiple TAP read or write operations". Correction is required. See MPEP § 608.01(b).

Claim Objections

2. Claims 8-14, 17-19, 22 and 24 are objected to because of the following informalities:

In claims 8-12: "said device access control" apparently should be "said device access control circuitry".

In claims 13 and 14: "said device access controller" apparently should be "said device access control circuitry".

In claim 17: "selectivley" apparently should be "selectively".

In claim 18: "one or more control signal" apparently should be "one or more control signals".

In claim 19: "said one of said control signals" apparently should be "one of said control signals".

In claim 22: "one of said control signal generated" apparently should be "and one of said control signals is generated".

In claim 24: "one of said control signal" apparently should be "one of said control signals".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 17-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 17, "written or read from the device without the need to repetitively cycle through *multiple shift operations*" is unclear to the point of being misdescriptive, as the specification clearly describes the use of "multiple shift operations" performed upon data during reading and writing under control of the inventive MAC circuit, *e.g.* "MAC 38 controls when the DREG 34 loads and shifts out memory data", "at the end of eight data bit shifts the 8-bit data word initially loaded into the target IC's DREG is shifted out of the DREG", and "the first bit of the next word can be shifted out on the next TCK shift cycle". The limitation is presumably a poorly-worded reference intended to correspond to the specification's observation that the MAC circuit operation "eliminates the need of having to repetitively cycle through *multiple TAP read or write operations*".

In claim 25, the "target interface circuit" is apparently incorrectly treated as an origin for data on the "bus" instead of a destination.

It is not clear how claims 30-36 can be distinguished from steps essential to the conventional arrangements described in connection with tables I and 2 of the disclosure.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-10, 15-22 and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,346,440 to Kyu *et al* (hereafter "Kyu").

Kyu discloses a data link controller (DLC) for a ring bus or other type of computer network. Kyu's DLC comprises a "data communication interface" "operable to communicate with a device", the device being a computer (not shown) on the network. Kyu's "bus circuitry for transferring data" is shown in Fig. 43, if not considered provided by a separate modem, for coupling to the network "bus". Kyu's "storage circuitry coupled to the device and to said bus" consists of shift registers of Kyu's RX and TX FIFOs (17, 18). Kyu's receiver circuitry (19, 20, 23, 24, 26, 27, 28, 29) serves as "interface circuitry operable to shift data between said bus and said storage circuitry".

Kyu's data bus interface and associated logic (10-16, 21, 22, 25) couples to the local host computer "device" and accordingly serves as "device access control circuitry operable to transfer data between said device and said storage circuitry responsive to a control signal".

Regarding claim 2, Kyu's local host computer "device" presumably "comprises a memory".

Regarding claim 6, Kyu's additional TX and RX data FIFO registers (#2, #3) serve as a "plurality of shift registers coupled to said bus circuitry".

Regarding claim 7, Kyu's "interface circuitry" transmits/receives network bus data from/to a selected one of the FIFOs (#1, #2, #3) and is thus "operable to shift data between said bus circuitry and a selected one of said shift registers".

Regarding claim 8, a status register (21, 22) of Kyu's "device access control circuitry" receives a "signal" from the "interface circuitry" of Kyu's controller for use in exchanging data between the local host device and Kyu's RX and TX FIFOs, by which Kyu's "device access control is operable to transfer data between said device and said storage circuitry".

Regarding claim 9, a TDRA/FC (Transmitter Data Register Available/Frame Complete) signal line of status register #1 (21) provides a bus transmission "pause signal" indication from Kyu's "interface circuitry" to the "device access control circuitry", for use in exchanging data between the local host device and Kyu's RX and TX FIFOs, by which Kyu's "device access control is operable to transfer data between said device and said storage circuitry responsive to a pause signal".

Regarding claims 10 and 22, a received '01111111' (Go Ahead) is a "predetermined sequence of data" that Kyu's "interface circuitry" is responsive to and that controls loop mode operation (Table 3, col. 33, lines 35-37, and col. 35 lines, 31-39), by which Kyu's "device access control is operable to transfer data between said device and said storage circuitry responsive to a predetermined sequence of data". Other candidates for a "predetermined sequence of data" include received supervisory frames, received data link management frames (col. 4, lines 55-60), a received frame delimiter and a 16-bit FCS result.

Regarding claims 15 and 16, a primary controller or station operable to transmit and receive data on Kyu's network bus serves as a "bus controller" (Fig. 6, etc.).

Regarding claims 17-19, one host computer "device" bus-cycle of Kyu's device is apparently sufficient to 8-bit data to be "written or read from the device without the need to repetitively cycle through multiple shift operations".

Regarding claim 20, data transmission between Kyu's local host computer "device" and Kyu's DLC is furthermore responsive to a "state machine" of Kyu's "interface circuitry", for example responsive to an error-free FCS result from the FCS check (20) and to a flag detector (27), both of which are part of a "state machine" as they include storage elements.

Regarding claim 21, when the "state machine" of Kyu's "interface circuitry" is idle it is in a "pause state".

Regarding claim 24, a received '01111111' (Go Ahead) is a "predetermined sequence of data" that is "received from an external device". Other candidates for a

"predetermined sequence of data" that is "received from an external device" include received supervisory frames, received data link management frames (col. 4, lines 55-60), a received frame delimiter and a 16-bit FCS result.

Regarding claims 25 and 26, in a loop network for Kyu's DLC, the DLC of a secondary station can be a "target interface circuit" for a sending or receiving operation when the primary station directs a message to the local host device, and intervening stations on the loop are "a plurality of interface circuits", each adding a 1-bit delay to a message. The process of sending data by Kyu's DLC of a secondary station targeted for a read operation by a primary station consists of "transferring data from the device into a register associated with the target interface circuit; shifting data from the register onto the bus; transferring additional data from the device into the register after the last data bit is shifted out of the register" (sic).

7. Claims 1-12, 14-20 and 22-36 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,768,190 to Giancarlo (hereafter "Giancarlo").

Giancarlo discloses a ring endpoint unit (40) transmitter-receiver for a ring bus fast packet switching network. Giancarlo's ring endpoint unit serves as a "data communication interface" that is "operable to communicate with a device", the "device" (100) being a computer on the network, for example. Giancarlo shows "bus circuitry for transferring data" (130, 132, 142) coupled to the network "bus" (30). Giancarlo also shows shift register "storage circuitry" (84, 88) that is "coupled to the device and to said bus", "interface circuitry" (134, 138, 140, 144, 146) that is "operable to shift data between said bus and said storage circuitry", and "device access control circuitry" (136,

85, 87, 90) that is "operable to transfer data between said device and said storage circuitry responsive to a control signal" .

Regarding claim 2, Giancarlo's "device" (100) presumably "comprises a memory".

Regarding claim 6, Giancarlo's "storage circuitry" comprises a "plurality of shift registers" (170, 172, 174) that are "coupled to said bus circuitry".

Regarding claim 7, Giancarlo's "interface circuitry" transmits/receives network bus data from/to a selected one of the shift registers of Giancarlo's "storage circuitry" and is thus "operable to shift data between said bus circuitry and a selected one of said shift registers".

Regarding claim 8, Giancarlo's "device access control circuitry" receives a "signal" from Giancarlo's "interface circuitry", such as the received packet address, by which Giancarlo's "device access control is operable to transfer data between said device and said storage circuitry".

Regarding claims 9 and 21, a "pause signal" from Giancarlo's "interface circuitry" to the "device access control circuitry", such as an indication of an empty pass through buffer (*i.e.* a pause in received data), is used in exchanging data between Giancarlo's computer "device" and Giancarlo's "storage circuitry", by which Giancarlo's "device access control is operable to transfer data between said device and said storage circuitry responsive to a pause signal".

Regarding claims 10 and 22, a received packet address is a "predetermined sequence of data" to which Giancarlo's "interface circuitry" is responsive, by which

Giancarlo's "device access control is operable to transfer data between said device and said storage circuitry responsive to a predetermined sequence of data". Other candidates for a "predetermined sequence of data" include received packet error check data.

Regarding claim 11, Giancarlo's "device access control" comprises a "first register (15), a "second register" (152) and "compare circuitry" (154).

Regarding claims 12, 14, 23 and 35, Giancarlo's "device access control" is "operable to transfer data between said device and said storage circuitry responsive to a signal indicating that a counter has counted to a predetermined number" (col. 7, lines 37-41), by means of Giancarlo's packet length register (158) and down counter (160).

Regarding claims 15 and 16, a checkpoint unit on Giancarlo's ring network can transmit and receive data and serves as a "bus controller coupled to said bus".

Regarding claims 17-19, one "device" bus-cycle of Giancarlo's "device" is apparently sufficient for multi-bit data to be "written or read from the device without the need to repetitively cycle through multiple shift operations".

Regarding claims 20 and 33, Giancarlo's "interface circuitry" comprises a "state machine" as it includes storage elements.

Regarding claims 24, 34 and 36, a received packet address is a "predetermined sequence of data" that is "received from an external device". Other candidates for a "predetermined sequence of data" that is "received from an external device" include received packet error check data.

Regarding claims 25 and 26, in a ring network for Giancarlo's endpoints, a destination endpoint is a "target interface circuit" and transmitting packet data necessarily involves "transferring data from the device into a register associated with the target interface circuit; shifting data from the register onto the bus; transferring additional data from the device into the register after the last data bit is shifted out of the register" (sic), and "sifting data sequentially through ones of said interface circuits".

Regarding claim 27, a selectable packet length, indicated by a type field (col. 6, lines 15-19), requires "counting the number of data bits transferred from the register", where the counting is in 16-bit units.

Regarding claim 28, Giancarlo's switching of the source of bus data from the transmit buffer to the pass through buffer requires an indication that "data stored in the register has been transferred to the bus".

Regarding claims 29, 30 and 32, Giancarlo's address recognition (154) at the "target" endpoint unit performs a step of "generating a control signal indicative of data reaching said target interface circuit" for "transferring data from a register associated with said target interface circuit to said device responsive to said signal".

Regarding claim 31, Giancarlo's packet data comprises a "predetermined value" that must be loaded into the pass through buffer registers of intervening endpoints in order to reach the intended destination endpoint.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Giancarlo.

Giancarlo uses a down-counter (160) preset by a length register and decremented until zero is reached, instead of an up-counter preset to zero and incremented until the length register value is reached. Official Notice is given that the equal suitability of up-counters and down-counters to a count-matching circuit was already well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to substitute an up-counter arrangement for the down-counter arrangement in the count-matching circuit shown by Giancarlo. Such a substitution would have been obvious because the equal suitability of up-counters and down-counters to a count-matching circuit was already well known.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen M. Baker
Primary Examiner
Art Unit 2133

smb